Intel® High Definition Audio Specification
Document Change Notification

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Company:	Intel Corporation		
Address:	1900 Prairie City Rd.		
City:	Folsom	State:	CA
Country:	USA	Zip:	95630

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Title: Correction to operation of Immediate Verb mechanism

Brief description of the functional changes:

The current implementations of the immediate verb command mechanism differs from the Intel® High Definition Audio Specification (HD Audio) version 1.0. As the currently shipping software/BIOSes implement the mechanism as built today, the specification will be updated to reflect the current implementations.

The discrepancy is that the ICS register in the specification is shown as read only, but it is actually writeable to allow for sending an immediate verb. The Immediate Command Status (ICS) register ICB (bit 0) is actually Read/Write and is used to cause a verb to be sent. It also can be forced to 0 in the case of a timeout condition.

Current Definition:

Sections 3.4 thru 3.4.3 of the Intel® High Definition specification version 1.0 defines:

3.4 Immediate Command Input and Output Registers

The Immediate Command Output and Immediate Command Input registers are optional registers which provide a Programmed I/O (PIO) interface for sending verbs and receiving responses from codecs. These registers can be implemented in platforms not suited for DMA command operations. If implemented, these registers must not be used at the same time as the CORB and RIRB command/response mechanisms, as the operations will conflict.

Offset 60h: Immediate Command Output Interface
Length: 4 bytes

Table 1. Immediate Command Output Interface

Bit	Type	Reset	Description
31:0	R/W	0's	**Immediate Command Write (ICW):** The value written into this register is sent out over the link during the next available frame. Software must ensure that the ICB bit in the Immediate Command Status register is clear before writing a value into this register or undefined behavior will result. Reads from this register will always return 0's.

Offset 64h: Immediate Response Input Interface
Length: 4 bytes

Table 2. Immediate Command Input Interface

Bit	Type	Reset	Description
31:0	R/W	0's	**Immediate Response Read (IRR):** The value in this register latches the last response to come in over the link. If multiple codecs responded in the same frame, there is no way to determine which response will be saved here, but the address of the codec is indicated in the ICRADD field of the Immediate Command Status register.

Offset 68h: Immediate Command Status
Length: 2 bytes

Table 3. Immediate Command Status

Bit	Type	Reset	Description
15:8	RsvdZ	0's	*Reserved*
7:4	RO	0's	**Immediate Response Result Address (IRRADD):** The address of the codec which sent the response currently latched into the Immediate Response Input register.
3	RO	0's	**Immediate Response Result Unsolicited (IRRUNSOL):** Indicates whether the response latched in the Immediate Response Input register is a solicited or unsolicited response.
2	RsvdZ	0's	*Reserved*
1	RW1C	0's	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IRR register. Software must clear this bit before issuing a new command by writing a one to it so that the software may determine when a new response has arrived.
0	RO	0's	**Immediate Command Busy (ICB):** This bit is a 0 when the controller can accept an immediate command. Software must wait for this bit to be 0 before writing a value in the ICW register. This bit will be clear (indicating "ready") when the following conditions are met: (1) the link is running, (2) the CORB is not active (CORBRP = CORBWP or CORBEN is not set), and (3) there is not an immediate command already in the queue waiting to be sent. Because software controls each of these conditions, this bit will not transition to a 1 after being read a 0 without explicit software operations to cause one of the above conditions to change.

New Definition:

Offset 60h: Immediate Command Output Interface
Length: 4 bytes

Table 4. Immediate Command Output Interface

Bit	Type	Reset	Description
31:0	R/W	0's	**Immediate Command Write (ICW):** The value written into this register is used as the verb to be sent out over the link when the ICB (ICS bit 0) is set to one (1). Software must ensure that the ICB bit in the Immediate Command Status register is clear before writing a value into this register or undefined behavior will result. ~~Reads from this register will always return 0's.~~

Offset 64h: Immediate Response Input Interface
Length: 4 bytes

Table 5. Immediate Command Input Interface

Bit	Type	Reset	Description
31:0	R/W	0's	**Immediate Response Read (IRR):** The value in this register latches the last response to come in over the link. If multiple codecs responded in the same frame, which one of the responses that will be saved is indeterminate. The codec's address for the response that was latched is indicated in the ICRADD field of the Immediate Command Status register if the ICRADD field is implemented.

Offset 68h: Immediate Command Status
Length: 2 bytes

Table 6. Immediate Command Status

Bit	Type	Reset	Description
15:8	RsvdZ	0's	*Reserved*
7:4	RO	0's	**Immediate Response Result Address (IRRADD):** The address of the codec which sent the response currently latched into the Immediate Response Input register. This field is optional.
3	RO	0's	**Immediate Response Result Unsolicited (IRRUNSOL):** Indicates whether the response latched in the Immediate Response Input register is a solicited or unsolicited response. This bit is optional.
2	RO	ICVER	**Immediate Command Version:** Indicates if the IRRADD field and IRRUNSOL bit are implemented. If ICVER is 0 then the IRRADD and IRRUNSOL are reserved. If ICVER is 1 then both IRRADD and IRRUNSOL are implemented.
1	RW1C	0's	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IRR register. Software must clear this bit before issuing a new command by writing a one to it so that the software may determine when a new response has arrived.

0	RW	0's	**Immediate Command Busy (ICB):** This bit is a 0 when the controller can accept an immediate command. Software must wait for this bit to be 0 before writing a value in the ICW register and may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Writing to 0 is not permissible if the CORB is active. This bit will be clear (indicating "ready") when the following conditions are met: (1) the link is running, (2) the CORB is not active (CORBRP = CORBWP or CORBEN is not set), and (3) there is not an immediate command already in the queue waiting to be sent. Writing this bit to 1 will cause the contents of the ICW register to be sent as a verb in the next frame. Once a response is received the IRV bit will be set and this bit will be cleared indicating ready to transmit another verb.

The steps for PIO operation are as follows:

(a) Software sets up the PIO verb to be sent out in the Immediate Command Output Register (ICW)
(b) Then software writes a "1" to Immediate Command Status ICB (bit 0 of ICS)
(c) HD Audio Controller sends out the PIO verb on the next frame and waits for response in following frame
(d) When response (in frame after PIO verb frame) is received the HD Audio controller sets the IRV (bit 1 of ICS) and clears ICB (bit 0 of ICS)
(e) Software polls for IRV (Bit 1 of ICS) being set, then the PIO verb response is read from the IRR register and the IRV is cleared by writing a 1 to it

In the case where IRV bit is not set after a long delay, software should implement a timeout condition where the software clears the ICB bit 0 and then polls until ICB bit 0 returns to zero.