Intel® High Definition Audio Specification
Document Change Notification

Date:	December 8, 2005		
Company:	Intel Corporation		
Address:	1900 Prairie City Rd.		
City:	Folsom	State:	CA
Country:	USA	Zip:	95630

Change Identification: **DCN No: HDA011-A**
Document Revision: Intel® High Definition Audio 1.0

Title: Clarification of CORB Read Pointer Reset

Brief description of the functional changes:

Current known implementations of HD Audio controllers implement CORB Read Pointer Reset differently than the HD Audio specification. The HD Audio specification is amended to reflect industry implementations. The specification shows bit 15 as write only and read as 0, but the actual implementation is Read/Write and requires the software to read back a 1 and then to clear the bit.

Example of existing hardware implementation:

18.2.17 CORBRP—CORB Read Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Ah Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15	**CORB Read Pointer Reset** — R/W. Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the Intel High Definition Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.

HD Audio 1.0 specification:

3.3.21 Offset 4Ah: CORBRP – CORB Read Pointer

Length: 2 bytes

Table 21. CORB Read Pointer

Bit	Type	Reset	Description
15	W	0	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0. The DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.

New Definition:

Offset 4Ah: CORBRP – CORB Read Pointer

Length: 2 bytes

Table 1. CORB Read Pointer

Bit	Type	Reset	Description
15	RW	0	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the controller. The hardware will physically update this bit to 1 when the CORB pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0, by writing a 0, and then read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted. ~~This bit will always be read as 0.~~
14:8	RsvP	0's	*Reserved*
7:0	R0	0's	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports up to 256 CORB entries (256 x 4 B = 1 KB) in the cyclic CORB buffer. This field may be read while the DMA engine is running.